|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | Q |  |
| 0 | 0 | 0 | 0 | A+B+C |
| 0 | 0 | 1 | 1 | A̅B̅C |
| 0 | 1 | 0 | 0 | A+B̅+C |
| 0 | 1 | 1 | 1 | A̅BC |
| 1 | 0 | 0 | 1 | AB̅C̅ |
| 1 | 0 | 1 | 1 | AB̅C |
| 1 | 1 | 0 | 0 | A̅+B̅+C |
| 1 | 1 | 1 | 0 | A̅+B̅+C̅ |
|  |  |  |  |  |
| POS: (A+B+C) (A+B̅+C) (A̅+B̅+C) (A̅+B̅+C̅) | | | | |
| SOP: (A̅B̅C) + (A̅BC) + (AB̅C̅) + (AB̅C) | | | | |

Since both circuits have the same number of gates, they are equally efficient unless the difference in power consumption, speed or efficiency between the AND and OR gates is not to be considered inconsequential. We can also infer that both circuits are probably of equal efficiency from the truth table since we have the same number of 0 and 1 outputs, however we also need to be mindful of a potential difference in the number of the required NOT gates.